Notice of Allowability	Application No.	Applicant(s)	
	10/015,414	FAN ET AL.	
	Examiner	Art Unit	
	Ly D Pham	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *09 September 2004*.

2. ☒ The allowed claim(s) is/are *5-7 and 9-11*.

3. ☒ The drawings filed on *12 December 2001* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

David Nelms
Supervisory Patent Examiner
Technology Center 2800

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Jiawei Huang (reg. no. 43,330) on September 9, 2004.

The application has been amended as follows:

Cancel claims 8 and 12.

Replace claims 5 and 9 with the following:

5. A method of erasing a non-volatile memory cell with a nitride tunneling layer, comprising:

providing a non-volatile memory cell comprising a substrate, a nitride tunneling layer disposed on the substrate, a charge trapping layer having hot electrons and disposed on the nitride tunneling layer, a dielectric layer disposed on the charge-trapping layer, a gate conductive layer disposed on the dielectric layer, a source region and a drain region disposed in the substrate adjacent to the nitride tunneling layer;

applying a first positive bias to the drain region;

applying a second positive bias to the gate conductive layer; and

grounding the source region and the substrate;

wherein the first positive bias and the second positive bias are both sufficient to inject hot electron holes into the charge-trapping layer through the nitride tunneling layer to combine with hot electrons in the charge-trapping layer for erasing the non-volatile memory cell.

9. A method of erasing a non-volatile memory cell with a nitride tunneling layer, comprising:

providing a non-volatile memory cell comprising a substrate, a nitride tunneling layer disposed on the substrate, a charge-trapping layer having hot electrons and disposed on and in direct contact with the nitride tunneling layer, a dielectric layer disposed on the charge-trapping layer, a gate conductive layer disposed on the dielectric layer, a source region and a drain region disposed in the substrate adjacent to the nitride tunneling layer;

applying a first positive bias to the drain region;

applying a second positive bias to the gate conductive layer; and

grounding the source region and the substrate;

wherein the first positive bias and the second positive bias are both sufficient to inject hot electron holes into the charge-trapping layer through the nitride tunneling layer to combine with hot electrons in the charge-trapping layer for erasing the non-volatile memory cell.

Allowable Subject Matter

2. Claims 5 – 7 and 9 – 11 are allowed.

3. The following is an examiner's statement of reasons for allowance:

The prior arts teach the method of erasing non-volatile memory cell, which applies appropriate biases to the drain, gate, source, and substrate regions to inject hot holes to combine with hot electrons in the charge-trapping layer for erasing the cell.

However, the prior arts did not teach the method above further applied in non-volatile memory cell being provided with a nitride tunneling layer disposed on the substrate, without a dielectric layer therebetween, and a charge-trapping layer disposed on the nitride tunneling layer for trapping hot carriers, for which structure the biases sufficient for erasing the cell are lower than those required for erasing memory cells of the same size.

4. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ly D Pham whose telephone number is 571-272-1793. The examiner can normally be reached on Mon-Fri, 8:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David Nelms
Supervisory Patent Examiner
Technology Center 2800

Ly Pham
September 9, 2004